**FPD LINK**

**Physical Layer Design Verification Checklist 00.06.03.401**

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# Change Control

|  |  |  |  |
| --- | --- | --- | --- |
| **Version** | **Date** | **Author CDSID** | **Changes / Remark** |
| AA | 6/21/2018 | hkadry | Initial Release |
| AB | 4/1/2019 | hkadry | Alignment with changes in version AB of ref[1] |
|  |  |  |  |

***Note:***

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# Introduction

## Scope

This document will serve as a design validation document to ensure all physical layer design requirements are met and implemented with appropriate evidence.

## Reference Documents

The requirements of the documents listed in the following table, form a part of this specification. The revision levels shown in the table were the latest at the time this Specification was written. In the event of a conflict between the requirements of this specification and these documents, the requirements in this document shall have precedence

|  |  |  |  |
| --- | --- | --- | --- |
| **Ref** | Document Number | File Name/Reference | Version |
| **1** | 00.06.03.004 | FPDLINKIII Physical Layer Specification | AB |
| **2** | FMC 1278 | Electromagnetic Compatibility Specification for Electrical/Electronic Components and Subsystems | Latest |
| **3** | 00.06.03.002 | Netcom Physical Layer Approved Components List | Latest |
| **4** | - | CSI-x Specification (MIPI Alliance) | Latest |
| **5** | - | USCAR 2 Specification | 6 |

Table 1: Reference Documents

## Definitions, Abbreviations and Acronyms

### Abbreviations

|  |  |
| --- | --- |
| PCB | Printed Circuit Board |
| FMC | Ford Motor Company |
| FPD LINK III | Flat Panel Display (FPD) Link III (TI Devices Trademark) |
| I2C | Inter - Integrated Circuit |
| ECU | Electronic Control Unit |
| EMC | Electromagnetic Compatibility |
| SerDes | Serializer/Deserializer |
| CMC | Common Mode Choke |
| WCA | Worst Case Analysis |

Table 2: Abbreviations and Acronyms

### Definitions

|  |  |
| --- | --- |
| Bus | A bus is a collection of one or more wires connecting two or more nodes. Each electronic device is equipped with a specific, standardised electronic interface in order to guarantee compatibility between exchanged binary items of information |
| Characteristic Impedance | The impedance along a transmission line, as a result of wave voltage to current ratio |
| Differential signalling | This is a method used to transmit data using two complimentary signals. |
| Imager | The Imager is the video source. It is connected to an FPD LINK III Serializer. The Imager and FPD Link III Serializer can be configured through the back channel. |
| Impedance Discontinuity | The impedance mismatch at a junction in an impedance controlled system |
| Insertion Loss | This defines the amount of signal lost during the journey of a signal from point A to point B. |
| Local Node | Local node is a designator given to the ECU that will provide power to another ECU over the data line, in this application coax (PoC) |
| Remote Node | Remote Node is a designator given to the ECU power by a local node over the data line, in this application coax (PoC) |
| Return Loss | This defines the amount of signal reflected back to the source after encountering an impedance mismatch in the medium. Return loss can contribute to insertion loss if significant |

Table 3: Definitions

## Overview Checklist

|  |  |  |
| --- | --- | --- |
|  | **Value** | **Comments** |
| **Review Date** |  |  |
| **Supplier** |  |  |
| **Vehicle/Model Year** |  |  |
| **Module Name** |  |  |
| **Module Part Number** |  |  |
| **Forward Channel Speed** |  |  |
| **Back Channel Speed** |  |  |
| **Serializer Part Number(s)** |  |  |
| **Deserializer Part Number(s)** |  |  |

Table 4: Overview Data

## Instructions

The following Documentation is required to complete and pass the Netcom Hardware Review:

* Bill of materials for all Netcom parts
* Drawings which allow inspection of the Layout for the Netcom circuits.
  + PCB Stack up
  + PCB Gerber Files
  + Signal Integrity analysis and simulation (Impedance, return loss, insertion loss, etc.)
  + Schematic of the relevant FPD Link III circuitry

*Please reference the attached checklist that will be filled out during the review*.

***AE hardware reviews can be completed by scheduling a 1 hour appointment with:***

*Gary O’Brien*

*System Engineering Architecture*

*EESE - Ford Motor Company*

*Building 5,3C003*

*Phone (313) 317-2346*

[*gobrien8@ford.com*](mailto:gobrien8@ford.com)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Name** | **Email** | **Telephone** |
| **Supplier Engineer** |  |  |  |
| **FMC D&R Engineer** |  |  |  |

Table 5: Contact Details

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Fail** | **Target Resolution Date** | **Pass With Exception** | **Pass** |
| **Overall Status** |  |  |  |  |
| **Comments** |  | | | |

Table 6: Overall Status

# Serializer and Deserializer IC Qualification Requirements

*Only applicable to IC supplier to qualify their Serializer and Deserializers*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Requirement | Evidence | Pass/Fail | Exception | Comments |
| PL\_AE\_02\_001 – EMC Testing   1. Verify the required EMC tests are compliant to ref [2]. |  |  |  |  |
| PL\_AE\_02\_002   1. Verify Supplier successfully qualified all provided interfaces to ref [2]. |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

# Circuit Requirements:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Requirement | Evidence | Pass/Fail | Exception | Comments |
| PL\_FPDLINK\_03\_001 –  FPD LINK III Differential Circuit Topology   1. Verify the SerDes ICs are on the approved list ref [3]. 2. Verify the board header connector is on the approved list ref [3]. 3. Verify the circuit components meet the specified requirements (e.g. Caps, etc.) 4. Provide evidence that schematic has been reviewed and approved by IC supplier. |  |  |  |  |
| PL\_FPDLINK\_03\_002/ PL\_FPDLINK\_03\_003 –  FPD LINK III Single Ended Circuit Topology   1. What is the data rate of the chipsets? 2. Verify the SerDes are on the approved list ref [3]. 3. Verify the board header connector is on the approved list ref [3]. 4. Verify the circuit components meet the specified requirements (Caps, etc.)? 5. Is the SerDes locally or remotely powered? 6. Which PoC was implemented? 7. Verify the PoC circuit components meet the specified requirements given the worst case remote node current draw (Ferrite Beads, Inductors, etc.) 8. Provide evidence that schematic has been reviewed and approved by IC supplier. |  |  |  |  |
|  |  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Requirement | Evidence | Pass/Fail | Exception | Comments |
| PL\_FPDLINK\_03\_004 –  FPD LINK IV Differential Circuit Topology   1. Verify the SerDes ICs are on the approved list ref [3]. 2. Verify the board header connector is on the approved list ref [3]. 3. Verify the circuit components meet the specified requirements (e.g. Caps, etc.) 4. Provide evidence that schematic has been reviewed and approved by IC supplier. |  |  |  |  |
| PL\_FPDLINK\_03\_005 –  FPD LINK IV Single Ended Circuit Topology   1. What is the data rate of the chipsets? 2. Verify the SerDes are on the approved list ref [3]. 3. Verify the board header connector is on the approved list ref [3]. 4. Verity the circuit components meet the specified requirements (Caps, etc.)? 5. Is the SerDes locally or remotely powered? 6. Which PoC was implemented? 7. Verify the PoC circuit components meet the specified requirements given the worst case remote node current draw (Ferrite Beads, Inductors, etc.) 8. Provide evidence that schematic has been reviewed and approved by IC supplier. |  |  |  |  |
|  |  |  |  |  |

# Hardware Design Requirements

| Requirement | Evidence | Pass/Fail | Exception | Comments |
| --- | --- | --- | --- | --- |
| PL\_FPDLINK\_04\_001 – SerDes IC Power Supply   1. Verify decoupling capacitor values are per IC supplier recommendation. 2. Verify ferrites are used per IC supplier recommendation. 3. Verify sufficient bulk capacitance is used at the IC supply pins per supplier recommendation. 4. Verify external core supplies meet IC supplier tolerances and a bulk capacitance ≥10uF is used at the supply output. 5. Verify the remote power provided from the local node is a regulated supply ≥9V and has current limiting ≤500mA. 6. Provide evidence that power strategy has been reviewed and approved by IC supplier. |  |  |  |  |
| PL\_FPDLINK\_04\_002 – IC Pins   1. Verify all IC pins are configured and used appropriately per latest data sheet. 2. Verify all unused pins are terminated correctly, as per supplier and Ford requirements. 3. Provide evidence of pin configuration review and approval by IC supplier. |  |  |  |  |
| PL\_FPDLINK\_04\_003 – Crystal and Reference Clock   1. Verify the crystal tolerance ≤50ppm for total of manufacturing, temperature and aging tolerances. 2. Provide evidence of load capacitance calculation. 3. Provide evidence or official plan for crystal characterization. |  |  |  |  |
| PL\_FPDLINK\_04\_003 –Reference Clock (Clock IC, Clock out, back channel clock)   1. Verify the clock tolerance ≤500ppm for total of manufacturing, temperature and aging tolerances. 2. Verify the clock jitter requirements meet the IC supplier specification. 3. Verify the Duty cycle meets the IC supplier specification. 4. Provide evidence of review and approval with IC supplier. |  |  |  |  |
| PL\_FPDLINK\_04\_004 – Reset/Power-Up   1. Verify the PDB pin timing meets IC supplier timing requirements. 2. Is a passive circuit used (e.g. RC) to set the PWDNB timing? If yes, provide the timing analysis with evidence of timing requirements being met? |  |  |  |  |
| PL\_FPDLINK\_04\_005 – Auto Configuration via Pin Strapping   1. Verify pin strapping for UART/I2C, Coax/Differential and Data rate are done in accordance to the chipset latest datasheet. 2. Provide evidence of pin strapping strategy has been reviewed and approved by IC supplier. |  |  |  |  |
| PL\_FPDLINK\_04\_006 – CSI-2 Interface ref[5]   1. Which CSI interface is implemented? 2. Verify no components are on CSI lines. 3. Verify the slew rate has been implemented according to IC supplier recommendation. 4. Verify the analysis of signal over-shoot and under-shoot has been provided for CSI signal lines to confirm that IC pin limits are not violated. 5. Verify no CSI lines have been daisy chained. |  |  |  |  |
| PL\_FPDLINK\_04\_007 – I2C Interface   1. Verify there is a pull-up resistor on each data line. 2. Verify the correct value is used based on the required speed. 3. Verify the correct address is implemented with pin strapping for addressing multiple SerDes |  |  |  |  |

# Board Layout Design Requirements

| Requirement | Evidence | Pass/Fail | Deviation | Comments |
| --- | --- | --- | --- | --- |
| PL\_FPDLINK\_05\_001 – PCB Stack up   1. How many layers is the PCB? 2. How many ground layers 3. How many power layers/islands? 4. Provide PCB stack-up drawing. |  |  |  |  |
| PL\_FPDLINK\_05\_002 – Return Path   1. Verify that all components for the high-speed circuits are connected to the same ECU ground. |  |  |  |  |
| PL\_FPDLINK\_05\_003 – Reference Plane   1. Verify there is an unobstructed reference plane (Ground) on the adjacent layer to the IC, components and layout. |  |  |  |  |
| PL\_FPDLINK\_05\_004 – SerDes Placement   1. Verify there are no ICs in the path between the board connector and SerDes IC. 2. Confirm that supplier has taken all reasonable steps to ensure the Dout+/Rin+ & Dout-/Rin- differential/single ended signal (trace length, components) from the connector to IC pins is ≤2 inches (50.8mm). |  |  |  |  |
| PL\_FPDLINK\_05\_005 – Differential (Dout+/Rin+ & Dout-/Rin-)   1. Confirm that supplier has taken all reasonable steps to ensure the characteristic impedance 100Ω±10%. 2. Confirm that supplier has taken all reasonable steps to ensure the differential pair trace length matched within ±5mils *(e.g. Ideally the differential pair are symmetrical, mirror copies of one another)* 3. Confirm impedance control is covered in PFMEA and included on the PCB print drawing. |  |  |  |  |
| PL\_FPDLINK\_05\_006 – Single Ended (Dout+/Rin+ and Dout-/Rin-)   1. Verify the separation between Dout+/Rin+ and Dout-/Rin-. 2. If ≤3x separation    1. Verify that Dout+/Rin+ and Dout-/Rin- are routed differentially with a characteristic impedance of 100Ω±10% and Dout-/Rin- is terminated at the connector.    2. Verify that Dout+/Rin+ is routed alone with a characteristic impedance of 50Ω±10% and Dout-/Rin- is terminated at the IC pin. 3. If ≥3x separation    1. Verify Dout+/Rin+ and Dout-/Rin- are each routed alone with a characteristic impedance of 50Ω±10% and Dout-/Rin- is terminated at the connector. |  |  |  |  |
| PL\_FPDLINK\_05\_006 – PCB Connector Footprint   1. Verify the connector layout analysis has been conducted with the final PCB stack up. Provide evidence of connector layout impedance. 2. Verify the footprint meets the soldering requirements *(solder volume for pin and paste)* as defined by the supplier, circuit board assembly process owners. |  |  |  |  |
| PL\_FPDLINK\_05\_007 – In Line Components   1. What are the in-line components package sizes? (*typically pad sizes for packages ≥0603 will require a reference plane not directly underneath the component pad*) 2. Confirm that supplier has taken all reasonable steps to ensure the pad impedance has been optimized to have a minimal effect on the trace characteristic impedance. 3. Confirm that supplier has taken all reasonable steps to ensure there are no unnecessary stub(s) for the inline components. |  |  |  |  |
| PL\_FPDLINK\_05\_008 – High Speed Trace Layout   1. How many transitions are present on the high-speed traces? Confirm that supplier has taken all reasonable steps to ensure ≤3 vias on the high-speed signal. 2. Verify ground via(s) are placed next to all transition via(s). 3. Upon which layer are the high-speed traces routed? List all layers from start to finish. 4. Verify high-speed traces are not routed across any ground/power splits. 5. Are there any test points? Are they necessary? Confirm that supplier has taken all reasonable steps to ensure test points are in line with the trace and symmetrical on the differential pairs. 6. Verify there are no 90-degree bends on high-speed traces. 7. Confirm that supplier has taken all reasonable steps to ensure    1. ≥2x (x=differential pair separation) separation between adjacent sets of high-speed differential signal pairs    2. ≥2x (x=single ended trace width) between single ended signals    3. ≥3x (x=differential pair separation) between a differential pair and single ended signal. 8. Confirm that supplier has taken all reasonable steps to ensure Inline capacitors are symmetrical on a differential pair 9. Confirm that supplier has taken all reasonable steps to ensure Inline capacitors are not aligned on adjacent non-differential high-speed signals. |  |  |  |  |
| PL\_FPDLINK\_05\_009 – Crystal Layout   1. Verify crystal supplier performed layout review. Provide evidence of approval from crystal supplier. 2. Verify no other signals are routed over the crystal circuit. 3. Confirm that supplier has taken all reasonable steps to ensure crystal traces are as short as possible, routed on the same layer and ground connections use multiple vias. |  |  |  |  |
| PL\_FPDLINK\_05\_010 – Reference Clock Trace Layout   1. Verity clock trace impedance matches the termination IC impedance within ±10%. 2. Verity the clock trace is routed ≥20x (x=trace width) from the edge of the board and ≥3x (x=trace width) from surrounding signal traces. |  |  |  |  |
| PL\_FPDLINK\_05\_011 – Magnetic Component Separation   1. Verify magnetic component separation is ≥2mm |  |  |  |  |
| PL\_FPDLINK\_05\_012 – Multi-Link Separation and Isolation   1. If multiple FPD LINKs exist on PCB, then verify the separation between the pairs is ≥3x (x=differential pair separation, single ended trace width) |  |  |  |  |
| PL\_FPDLINK\_05\_013 – CSI-x Signal Lines   1. Confirm that supplier has taken all reasonable steps to ensure differential CSI signals are routed with 100Ω±10% impedance and matched in length within ±1%. *(Ideally differential pairs are symmetrical mirrors copies of one another)* 2. Verify flight time is ≤2ns. 3. Supplier must provide signal integrity analysis for FMC review.    1. Verify return loss ≤ -13 dB at the operating frequency.    2. Verify Insertion loss ≤ 2 dB at the operating frequency    3. Verify crosstalk isolation of 30dB or better from surrounding signals or provide detailed signal integrity confirmation for victim signal in presence of offending crosstalk level.    4. Verify analysis includes all PCB manufacturing tolerances. 4. Confirm impedance control is covered in PFMEA and included on the PCB print drawing. |  |  |  |  |
| PL\_FPDLINK\_05\_014 – Parallel Data Signal Lines   1. Confirm that supplier has taken all reasonable steps to ensure single ended parallel signals are routed with 50Ω±10% impedance and are matched in length within ± 1%. 2. Supplier must provide signal integrity analysis for FMC review.    1. Verify return loss ≤ -13 dB at the operating frequency.    2. Verify Insertion loss ≤ 2 dB at the operating frequency    3. Verify crosstalk isolation of 30dB or better from surrounding signals or provide detailed signal integrity confirmation for victim signal in presence of offending crosstalk level.    4. Verify analysis includes all PCB manufacturing tolerances. 3. Confirm impedance control is covered in PFMEA and included on the PCB print drawing. |  |  |  |  |

# SerDes PCB Circuit S-Parameter Requirements

| Requirement | Evidence | Pass/Fail | Deviation | Comments |
| --- | --- | --- | --- | --- |
| PL\_FPDLINK\_06\_001 –FPD LINK III Signal Board Return Loss   1. Verify the PCB circuit (with all components) meets the return loss budget. 2. Provide simulation and/or measurement report and touch tone files showing evidence of compliance. 3. Verify the simulation or measurement incorporates all tolerances. (temperature and manufacturing) 4. Verify that the simulation model properly incorporates the IC pads and their adjacent ground planes 5. Verify that the DVP and PVP contain PCB measurement of ENET return loss against limit line is ref[1] |  |  |  |  |
| PL\_FPDLINK\_06\_002 – FPD LINK III Board Signal Insertion Loss   1. Verify the PCB circuit (with all components) meet the insertion loss budget. 2. Provide simulation and/or measurement report and touch tone files showing evidence of compliance. 3. Verify the simulation or measurement incorporates all tolerances. (temperature and manufacturing) 4. Verify that the DVP and PVP contain PCB measurement of ENET insertion loss against limit line is ref[1] |  |  |  |  |

| Requirement | Evidence | Pass/Fail | Deviation | Comments |
| --- | --- | --- | --- | --- |
| PL\_FPDLINK\_06\_003 –FPD LINK IV Signal Board Return Loss   1. Verify the PCB circuit (with all components) meets the return loss budget. 2. Provide simulation and/or measurement report and touch tone files showing evidence of compliance. 3. Verify the simulation or measurement incorporates all tolerances. (temperature and manufacturing) 4. Verify that the simulation model properly incorporates the IC pads and their adjacent ground planes 5. Verify that the DVP and PVP contain PCB measurement of ENET return loss against limit line is ref[1] |  |  |  |  |
| PL\_FPDLINK\_06\_004 – FPD LINK IV Board Signal Insertion Loss   1. Verify the PCB circuit (with all components) meet the insertion loss budget. 2. Provide simulation and/or measurement report and touch tone files showing evidence of compliance. 3. Verify the simulation or measurement incorporates all tolerances. (temperature and manufacturing) 4. Verify that the DVP and PVP contain PCB measurement of ENET insertion loss against limit line is ref[1] |  |  |  |  |

| Requirement | Evidence | Pass/Fail | Deviation | Comments |
| --- | --- | --- | --- | --- |
| PL\_FPDLINK\_06\_005–PoC Impedance Characteristics   1. Verify supplier has performed Impedance vs. Frequency analysis, unloaded and load max current on the PoC from the backchannel frequency to the forward channel frequency and present impedance data to FMC engineer. Supplier must determine impedance requirement from IC supplier.   (e.g. 933/934 ≥1kΩ, 953/954 ≥2kΩ) |  |  |  |  |
|  |  |  |  |  |